ABSTRACT / ZUSAMMENFASSUNG / ABREGE

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In this invention, by offering specific array-end structures and their fabrication method, the three resistive layers of diffusion bit line (003), control gate (042) and word gate (040) polysilicons, where control gate (042) polysilicon can run on top of the diffusion bit line (003), are most effectively stitched with only three layers of metal lines (061,071,081) keeping minimum metal pitches. The stitching method can also incorporate a bit diffusion select transistor and/or a control gate line select transistor. The purpose of the select transistors may be to reduce the overall capacitance of the bit line or control gate line, or to limit the disturb conditions that a grouped sub-array of cells may be subjected to during program and/or erase.